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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.     | CONFIRMATION NO.       |
|--|-------------|----------------------|-------------------------|------------------------|
| 10/840,206   | 05/05/2004  | Ian Chesal           | 015114-074300US         | 7267                   |
| 26059 7590 05/30/2007<br>TOWNSEND AND TOWNSEND AND CREW LLP/ 015114<br>TWO EMBARCADERO CENTER<br>8TH FLOOR<br>SAN FRANCISCO, CA 94111-3834 |             |                      | EXAMINER<br>SIEK, VUTHE |                        |
|  |             |                      | ART UNIT<br>2825        | PAPER NUMBER           |
|  |             |                      | MAIL DATE<br>05/30/2007 | DELIVERY MODE<br>PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/840,206

Applicant(s)

CHESAL ET AL.

Examiner

Vuthe Siek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8, 10-17, 19 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-17, 19 and 20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This office action is in response to application 10/840,206 filed on 5/5/2004.

Claims 1-8, 10-17 and 19-20 remain pending in the application, where claims 9 and 18 are canceled.

2. Note that the indicated allowable subject matter has been withdrawn in view of newly found art in view of new ground of rejection as followed.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8, 11-17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aleksic et al. (5,995,736).

5. As to claim 1 and 12, Aleksic et al. teach substantially the same claimed invention of editing a file describing a circuit design so that HDL code in the file is compatible with a new programmable logic IC (Fig. 2, 3, 4, 5, 6 and 7) comprising locating black box declarations and black box instances in the file (file 34 in Fig. 2; file 34 in Fig. 3; file 82 in Fig. 5; black box declarations and black box instances in Fig. 6A-E); gathering information about the black box declarations and instances, wherein a black represents a circuit block within a circuit design and the information gathered represents one or more attributes of a circuit represented by a black box (register file contains all of pertinent register information about devices being developed including its

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offset, access permission, size, and field specification; see at least summary; col. 3 lines 53-67; col. 4 lines 1-17; col. 5 lines 9-67; col. 6 lines 15-67; col. 8 lines 8-24); editing the black box declarations to create equivalent black box declarations that are compatible with the new programmable logic IC using the information (at least described in col. 8); editing the black box instances to create equivalent black box instances that compatible with the new programmable logic IC using the information (at least see col. 8); and generating a detailed report that indicated where the black box declarations and instances were found in the code and the equivalent declarations and instances that the black boxes were replaced with and the codes are stored in register file (at least see Fig. 5 where report is generated, the register is modified as needed).

6. As to claims 2 and 13, the limitation of generating a warning if an equivalent black box compatible with the new programmable logic IC cannot be located for one of the black box instances or declarations is inherently within the art (see at least Fig. 5).

7. As to claims 3 and 14, Aleksic et al. teach automatically any dangling signals or unused ports in the equivalent black box instances to pre-selected terminals (at least see Fig. 5)..

8. As to claims 4 and 15, Aleksic et al. teach determining a number of input ports and output ports for each of the black box declarations (Fig. 6A-E; col. 9-10).

9. As to claims 5 and 16, Aleksic et al. each gathering information about the black box instances comprising identifying input signals coupled to each input port of the black box instances, and identifying output signals coupled to each output port of the black box instances (Fig. 5, 6A-E; col. 9-10).

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10. As to claims 6 and 17, Aleksic et al. teach gathering information about the black box declarations comprising determining a function performed by each of the black box declarations (Fig. 5, 6A-E).

11. As to claim 8, Aleksic et al. teach stopping and restarting the codes that implement a design conversion process for the circuit design without having to reparse the design conversion process from the beginning and saving a state of the design conversion to memory (at least see col. 8; Fig. 5).

12. As to claim 11, Aleksic et al. teach identifying blocks of code that do not have body definition as black box declarations (at least see Fig. 6A-E; col. 9-10).

13. As to claim 20, Aleksic et al. teach generating a detailed report (at least Fig. 5).

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Aleksic et al. (5,995,736) in view of Khakzaki et al. (US 2005/0114818 A1).

16. As to claim 7, Aleksic et al. teach written source code in HDL, but suggest any other code can be used. Khakzaki et al. teach using TCL scripts written in TCL code. The command processor uses a TCL command language interpreter to allow the user the capability to fully configure and change the contents of all menu, button and keyboard accelerations at any time during run time. In addition, Khakzaki et al. teach

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each designer can use TCL scripts to create a custom environment, where the custom user environment can then be loaded on command and without logging off (0026-0033).

With these motivations, it would have obvious to practitioners in the art at the time the invention was made to write source code in TCL code that is executed as a script sourced through an executable in a synthesis tool.

17. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Aleksic et al.(5,995,736) in view of Sanders (6,536,017 B1).

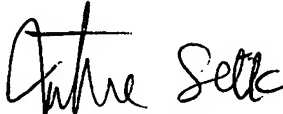
18. As to claims 10 and 19, Aleksic et al. do not teach timing constraints during conversion process. Sanders teach generating constraint file (timing constrains) during conversion process (col. 5 lines 45-67; col. 6 lines 1-26) in order to optimize the circuit design. With that motivation, it would have been obvious to practitioners in the art at the time the invention was made to converting timing constraints associated with the circuit design to be compatible with the new programmable logic IC.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
VUTHE SIEK  
PRIMARY EXAMINER